AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

1. (currently amended) A method of passivating trap sites in a semiconductor device, said method comprising:

fabricating a semiconductor device on a semiconductor substrate;

electrically stressing the semiconductor device to remove non-passivating species from trap sites; and

annealing said electrically stressed semiconductor device with a passivation process to passivate said trap sites.

2. (currently amended) The method as in claim 1, wherein said semiconductor device is a transistor comprising a source, a gate and a drain, and wherein said step of electrically stressing comprises applying a voltage potential to said drain while the gate is negatively ~~pulsing said gate~~ pulsed, said voltage potential being less than the semiconductor device's breakdown potential

Claims 3-4 (cancelled).

5. (original) The method as in claim 2, wherein said applied voltage potential is at an operational supply voltage of the semiconductor device.

6. (original) The method as in claim 1, wherein said semiconductor device is a transistor comprising a source, a gate, and a drain, and wherein said step of electrically stressing creates a high electric field at said source.

7. (original) The method as in claim 6, wherein said step of electrically stressing comprises applying peak-substrate current conditions.

8. (currently amended) The method as in claim 7, further comprising driving said transistor in a bipolar mode when the applied gate voltage is approximately Vd/2, where Vd is the drain voltage.

9. (currently amended) The method as in claim 1, wherein said semiconductor device is a transistor further comprising a source, a gate, and a drain, and wherein said step of electrically stressing ~~produce~~ produces hot carriers near a drain overlap region.

10. (currently amended) The method as in claim 9, wherein said step of electrically stressing comprises applying peak-substrate current conditions ~~when Vd is approximately high, Vg is approximately at least above threshold, and Vt is approximately Vd/3~~ where Vg is approximately Vd/2, and Vg is the gate voltage and Vd is the drain voltage.

11. (cancelled)

12. (cancelled).

13. (original) The method as in claim 9, wherein said transistor has trap sites, and wherein said hot carriers remove hydrogen from the trap sites.

14. (original) The method as in claim 1, wherein said semiconductor device is a transistor comprising a source, a gate, and a drain, and wherein said step of electrically stressing produce hot carriers.

15. (original) The method as in claim 14, wherein said transistor has trap sites, and wherein said hot carriers remove hydrogen from the trap sites.

16. (original) The method as in claim 1, wherein said semiconductor device is a transistor comprising a source, a gate, and a drain, and wherein said step of electrically stressing produce hot carriers near a source overlap region.

17. (original) The method as in claim 16, wherein said step of electrically stressing comprises applying peak-substrate current conditions.

18. (currently amended) The method as in claim 17, wherein said peak-substrate ~~gate voltage~~ current conditions occur ~~when Vd is approximately high, and Vg~~ is

~~negative with a negative drain pulse applied to the gate~~ where Vg is approximately Vd/2, and Vd is a negative drain voltage and Vg is the gate voltage.

Claims 19-20 (cancelled).

21. (original) The method as in claim 16, wherein said transistor has trap sites, and wherein said hot carriers remove hydrogen from the trap sites.

22. (original) The method as in claim 1, wherein said step of electrically stressing is effected at a temperature less than approximately 650°C.

23. (original) The method as in claim 1, wherein said semiconductor substrate is a silicon-on-insulator substrate.

24. (currently amended) The method as in claim 1, wherein said passivation [annealing] process is a deuterium passivation process.

25. (currently amended) The method as in claim 1, wherein said semiconductor device further ~~including~~ comprises a gate dielectric layer ~~on~~ formed over said substrate, said gate dielectric forming an interface with said substrate, and said step of electrically stressing ~~includes~~ further comprises electrically stressing the interface prior to said step of annealing.

26. (cancelled).

27. (currently amended) The method as in claim 25, wherein said interface has trap sites, and wherein said step of electrically stressing ~~produce~~ produces hot carriers.

28. (original) The method as in claim 27, further comprising removing hydrogen from said trap sites with the hot carriers.

29. (currently amended) The method as in claim 1, wherein said semiconductor device further ~~including~~ comprises a buried oxide layer formed in said substrate, said buried oxide layer forming an interface with said substrate, and said step of electrically stressing ~~includes~~ further comprises electrically stressing the interface prior to said step of annealing.

30. (currently amended) The method as in claim 29, wherein said interface has trap sites, and wherein said step of electrically stressing ~~produce~~ produces hot carriers.

31. (original) The method as in claim 30, further comprising removing hydrogen from said trap sites with the hot carriers.

32. (currently amended) The method as in claim 1, wherein said semiconductor device further ~~including~~ comprises oxide isolation regions in said substrate,

said oxide isolation regions and said substrate forming an interface, and said step of electrically stressing ~~includes~~ further comprises electrically stressing the interface prior to said step of annealing.

33. (original) The method as in claim 32, wherein said oxide isolation regions are shallow trench isolation regions, and wherein said shallow trench isolation regions have trap sites.

34. (original) The method as in claim 33, wherein said trap sites are located along the oxide isolation region sidewalls.

35. (currently amended) The method as in claim 32, wherein said interface has trap sites, and wherein said step of electrically stressing ~~produce~~ produces hot carriers.

36. (original) The method as in claim 35, further comprising removing hydrogen from said trap sites with the hot carriers.

37. (currently amended) The method as in claim 1, wherein said semiconductor device further ~~including~~ comprises shallow trench isolation regions and a buried oxide layer in said substrate, said shallow trench isolation regions forming interfaces with said buried oxide layer and said substrate, and said step of electrically stressing

~~includes~~ further comprises electrically stressing said interfaces prior to said step of annealing.

38. (currently amended) The method as in claim 37, wherein said interfaces have trap sites, and wherein said step of electrically stressing ~~produce~~ produces hot carriers.

39. (original) The method as in claim 38, further comprising removing hydrogen from said trap sites with the hot carriers.

40. (currently amended) A method of fabricating an integrated circuit, said method comprising the steps of:

fabricating a transistor device on a silicon-on-insulator substrate, said transistor comprising a source, a gate, and a drain;

electrically stressing said transistor to remove hydrogen occupying trap sites in the transistor; and

annealing said electrically stressed transistor with a passivation process to passivate said trap sites.

41. (currently amended) The method as in claim 40, wherein said step of electrically stressing comprises applying a voltage potential to said drain while the gate is negatively ~~pulsing said gate~~ pulsed, wherein said voltage potential is less than the transistor's breakdown potential.

Claims 42-43 (cancelled).

44. (original) The method as in claim 41, wherein said applied voltage potential is at an operational supply voltage of the transistor.

45. (original) The method as in claim 40, wherein said step of electrically stressing creates a high electric field at said source.

46. (currently amended) The method as in claim 45, wherein said step of electrically stressing further comprises applying peak-substrate current conditions where the gate voltage is approximately Vd/2, and Vd is the drain voltage.

47. (cancelled).

48. (currently amended) The method as in claim 40, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a drain overlap region in said transistor.

49. (currently amended) The method as in claim 48, wherein said step of electrically stressing further comprises applying peak-substrate current conditions ~~when Vd is approximately high, Vg is approximately at least above threshold, and Vt is~~

~~approximately Vd/3~~ where Vg is approximately Vd/2, and Vg is the gate voltage and Vd is the drain voltage.

Claims 50-51 (cancelled).

52. (original) The method as in claim 48, further comprising removing hydrogen from said trap sites with the hot carriers.

53. (original) The method as in claim 40, wherein said step of electrically stressing produce hot carriers.

54. (original) The method as in claim 53, further comprising removing hydrogen from said trap sites with the hot carriers.

55. (currently amended) The method as in claim 40, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a source overlap region in said transistor.

56. (currently amended) The method as in claim 55, wherein said step of electrically stressing further comprises applying peak-substrate current conditions.

57. (currently amended) The method as in claim 56, wherein said peak-substrate ~~gate voltage~~ current conditions occur ~~when Vd is approximately high, and Vg is negative with a negative drain pulse applied to the gate~~ where Vg is approximately Vd/2, and Vd is a negative drain voltage and Vg is the gate voltage.

Claims 58-59 (cancelled).

60. (original) The method as in claim 55, further comprising removing hydrogen from said trap sites with the hot carriers.

61. (original) The method as in claim 40, wherein said step of electrically stressing is effected at a temperature of less than approximately 650°C.

62. (currently amended) The method as in claim 40, wherein said passivation [[annealing]] process is a deuterium passivation process.

63. (previously amended) A method of fabricating a semiconductor device, said method comprising:

forming a transistor on a semiconductor substrate, said transistor having a source, a gate, a drain, and a plurality of trap sites, with hydrogen atoms occupying at least one of said trap sites;

removing said at least one hydrogen atom from said trap sites by electrically stressing said transistor; and

providing deuterium atoms which bond to said trap sites after said at least one hydrogen atom is removed.

64. (currently amended) The method as in claim 63, wherein said step of electrically stressing comprises applying a voltage potential to said drain while the gate is negatively ~~pulsing said gate~~ pulsed, wherein said voltage potential is less than the transistor's breakdown potential.

Claims 65-66 (cancelled).

67. (original) The method as in claim 64, wherein said applied voltage potential is at an operational supply voltage of the transistor.

68. (currently amended) The method as in claim 63, wherein said step of electrically stressing further ~~comprising~~ comprises creating a high electric field at said source.

Claims 69-70 (cancelled).

71. (currently amended) The method as in claim 63, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a drain overlap region in said transistor.

72. (currently amended) The method as in claim 71, wherein said step of electrically stressing further comprises applying [[near]] peak-substrate ~~gate voltage~~ current conditions.

73. (currently amended) The method as in claim 72, wherein said peak-substrate ~~gate voltage~~ current conditions occur ~~when Vd is approximately high, Vg is approximately at least about threshold, and Vt is approximately Vd/3~~ where Vg is approximately Vd/2, and Vd is the drain voltage and Vg is the gate voltage.

Claims 74-75 (cancelled).

76. (currently amended) The method as in claim 63, wherein said step of electrically stressing ~~produce~~ produces hot carriers.

77. (original) The method as in claim 76, further comprising removing at least one hydrogen atom from said trap sites with the hot carriers.

78. (currently amended) The method as in claim 63, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a source overlap region in said transistor.

79. (currently amended) The method as in claim 78, wherein said step of electrically stressing further comprises applying peak-substrate current conditions.

80. (currently amended) The method as in claim 79, wherein said peak-substrate ~~gate voltage~~ current conditions occur ~~when Vd is approximately high, and Vg is negative with a negative drain pulse applied to the gate~~ where Vg is approximately Vd/2, and Vd is a negative drain voltage and Vg is the gate voltage.

Claims 81-82 (cancelled).

83. (original) The method as in claim 78, further comprising removing at least one hydrogen atom from said trap sites with the hot carriers.

84. (original) The method as in claim 63, wherein said step of electrically stressing is effected at a temperature of less than approximately 650°C.

85. (original) The method as in claim 63, wherein said deuterium atoms are provided in a deuterium passivation process.

86. (previously amended) A method of reducing the number of trap sites in a semiconductor device, said method comprising:

forming a transistor on a semiconductor substrate, said transistor having a source, a gate, a drain, and a plurality of trap sites with non-passivating species occupying at least one of said trap sites;

removing said at least one non-passivating species from said trap sites by electrically stressing said transistor; and

providing at least one passivating species that occupies said trap sites.

87. (currently amended) The method as in claim 86, wherein said step of electrically stressing comprises applying a voltage potential to said drain while the gate is negatively ~~pulsing said gate~~ pulsed, wherein said voltage potential is less than the transistor's breakdown potential.

Claims 88-89 (cancelled).

90. (original) The method as in claim 87, wherein said applied voltage potential is at an operational supply voltage of the transistor.

91. (currently amended) The method as in claim 86, wherein said step of electrically stressing further comprises creating a high electric field at said source.

Claims 92-93 (cancelled).

94. (currently amended) The method as in claim 86, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a drain overlap region in said transistor.

95. (currently amended) The method as in claim 94, wherein said step of electrically stressing further comprises applying [[near]] peak-substrate ~~gate voltage~~ current conditions.

96. (currently amended) The method as in claim 95, wherein said peak-substrate ~~gate voltage~~ current conditions occur ~~when Vd is approximately high, Vg is approximately at least about threshold, and Vt is approximately Vd/3~~ where Vg is approximately Vd/2, and Vd is the drain voltage and Vg is the gate voltage.

97. (cancelled).

98. (original) The method as in claim 94, further comprising removing at least one non-passivating species from said trap sites with the hot carriers.

99. (currently amended) The method as in claim 86, wherein said step of electrically stressing ~~produce~~ produces hot carriers.

100. (original) The method as in claim 99, further comprising removing at least one non-passivating species from said trap sites with the hot carriers.

101. (currently amended) The method as in claim 86, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a source overlap region in said transistor.

102. (currently amended) The method as in claim 101, wherein said step of electrically stressing further comprises applying peak-substrate current conditions.

103. (currently amended) The method as in claim 102, wherein said peak-substrate ~~gate voltage~~ current conditions occur ~~when Vd is approximately high, and Vg is negative with a negative drain pulse applied to the gate~~ where Vg is approximately Vd/2, and Vd is a negative drain voltage and Vg is the gate voltage.

Claims 104-105 (cancelled).

106. (original) The method as in claim 101, further comprising removing at least one non-passivating species from said trap sites with the hot carriers.

107. (original) The method as in claim 86, wherein said step of electrically stressing is effected at a temperature of less than approximately 650°C.

108. (original) The method as in claim 86, wherein said at least one passivating species is deuterium.

109. (previously amended) The method as in claim 108, wherein said deuterium is provided by a deuterium passivation process.

110. (cancelled).

111. (currently amended) A method of passivating trap sites in a semiconductor device, said method comprising:

forming a transistor having a plurality of trap sites, with non-passivating species occupying at least one of said trap sites;

removing said at least one non-passivating species from the trap sites by electrically stressing the transistor, wherein said step of electrically stressing comprises applying a voltage potential to said drain and applying a negative pulse to said gate; and

providing at least one passivating species which ~~bond~~ bonds to said trap sites after said at least one non-passivating species is removed.

112. (cancelled).

113. (currently amended) The method as in claim [[112]] 111, wherein said applied voltage potential is ~~significantly~~ less than the ~~device~~ transistor's breakdown potential ~~that is applied to the drain~~.

114. (original) The method as in claim 111, wherein said applied voltage potential is at an operational supply voltage of the transistor.

115. (currently amended) The method as in claim 111, wherein said step of electrically stressing further comprises creating a high electric field at said source.

116. (currently amended) The method as in claim 115, wherein said step of electrically stressing further comprises applying peak-substrate current conditions.

117. (currently amended) The method as in claim 116, further comprising driving said transistor in a bipolar mode when the gate voltage is approximately Vd/2, and Vd is the drain voltage.

118. (currently amended) The method as in claim 111, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a drain overlap region in said transistor.

119. (currently amended) The method as in claim 118, wherein said step of electrically stressing further comprises applying peak-substrate current conditions ~~when Vd is approximately high, Vg is approximately at least above threshold, and Vt is approximately Vd/3~~ where Vg is approximately Vd/2, Vg is the gate voltage and Vd is the drain voltage.

Claims 120-121 (cancelled).

122. (original) The method as in claim 118, further comprising removing at least one non-passivating species from said trap sites with the hot carriers.

123. (currently amended) The method as in claim 111, wherein said step of electrically stressing ~~produce~~ produces hot carriers.

124. (original) The method as in claim 123, further comprising removing at least one non-passivating species from said trap sites with the hot carriers.

125. (currently amended) The method as in claim 111, wherein said step of electrically stressing ~~produce~~ produces hot carriers near a source overlap region in said transistor.

126. (currently amended) The method as in claim 125, wherein said step of electrically stressing further comprises applying peak-substrate current conditions.

127. (currently amended) The method as in claim 126, wherein said peak-substrate ~~gate voltage~~ current conditions occur ~~when Vd is approximately high, and Vg is negative with a negative drain pulse applied to the gate~~ where Vg is approximately Vd/2, and Vd is a negative drain voltage and Vg is the gate voltage.

Claims 128-129 (cancelled).

130. (original) The method as in claim 125, further comprising removing at least one non-passivating species from said trap sites with the hot carriers.

131. (original) The method as in claim 111, wherein said step of electrically stressing is effected at a temperature of less than approximately 650°C.

132. (original) The method as in claim 111, wherein said at least one passivating species is deuterium.

133. (previously amended) The method as in claim 132, wherein said deuterium is provided by a deuterium passivation process.